PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-066406
(43)Date of publication of application : 10.03.1995

(51)Int.CI. H01L 29/78
H01L 21/336
H01L 21/28

(21)Application number : 05-210584
(22)Date of filing : 25.08.1993

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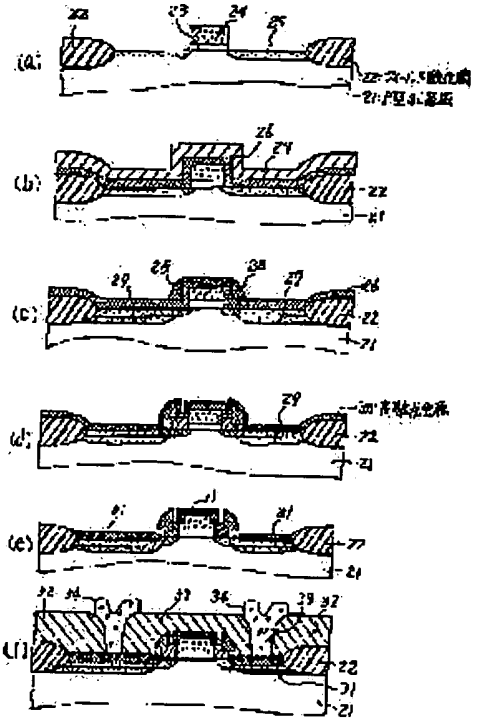
(72)Inventor : IDA JIRO

(54) SELF-ALIGNED SILICIDE MOSFET AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To restrain the increase of gate resistance in accordance with the reduction of gate size, and realize the high speed operation of a circuit.
CONSTITUTION: In a self-aligned silicide MOSFET, high melting point metal silicide 31 is formed in at least a part of both side surfaces of a gate electrode 24 and at least a part of the lower portion of a side wall 28 of the gate electrode 24.



LEGAL STATUS

[Date of request for examination] 24.08.1999
[Date of sending the examiner's decision of rejection] 26.06.2001
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] Salicide type MOSFET characterized by providing the refractory-metal silicide in which the both-sides side of a gate electrode is formed in part at least.
[Claim 2] Salicide type MOSFET according to claim 1 characterized by providing the refractory-metal silicide in which the lower part of the sidewall insulator layer of the aforementioned gate electrode is formed in part at least.
[Claim 3] (a) The process which deposits an oxide film on the whole surface after gate electrode formation, and the process which deposits a nitride all over (b) and forms a nitride sidewall by anisotropic etching, (c) The process which **********s so that a part of both-sides side of the aforementioned gate electrode may expose the aforementioned oxide film and a part of silicon substrate under a nitride sidewall may be exposed, (d) The manufacture method of Salicide type MOSFET characterized by giving the process which deposits a refractory metal on the whole surface, and the process which performs (e) silicide-ized reaction and removes an unreacted refractory metal.
[Claim 4] (a) The manufacture method of Salicide type MOSFET characterized by giving the process which deposits an insulator layer on the whole surface after gate electrode formation, the process which etches until a part of gate electrode both-sides side is exposed with (b) anisotropic etching, the process which deposits a refractory metal all over (c), and the process which performs (d) silicide-ized reaction and removes an unreacted refractory metal.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the structure and its manufacture method of Salicide type MOSFET.
[0002]
[Description of the Prior Art] In order for the gate length to become short and to suppress a short channel effect as MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is reduction-ized, the junction depth Xf of a source drain field must be made shallow. Since gate length becomes short, the on resistance of MOSFET falls and Xj becomes shallow by one side, sheet resistance of a source drain increases.
[0003] Therefore, in MOSFET of a submicron field, it becomes impossible for sheet resistance of a source drain to ignore to the on resistance of MOSFET, and gate length becomes remarkable [the problem to which the driving force of MOSFET falls by parasitism resistance of a source drain field]. To such a problem, a source drain and the gate are silicide-ized to self-alignment, and there is a salicide process which lowers sheet resistance.
[0004] Titanium Salicide is shown for Salicide type MOSFET and the process conventionally used for drawing 2 in an example.
(1) First, as shown in drawing 2 (a), usually form the gate electrode 3, a sidewall 4, and the source drain layer 5 after forming the field oxide film 2 on the semiconductor substrate 1 according to a manufacturing process.
[0005] (2) Next, as shown in drawing 2 (b), deposit the Ti film 6 on the whole surface.
(3) Next, make silicide 7-ization cause in the place where the source drain, and the silicon layer and the Ti film 6 of the gate have touched by annealing for about 10 seconds at 700 degrees C, as shown in drawing 2 (c). Then, selective etching removes unreacted Ti on the field oxide film 2 and a sidewall 4. Then, silicide low resistance-ized annealing for about 10 seconds is performed at 900 degrees C.
[0006] (4) After that, usually, according to a process, as shown in drawing 2 (d), an interlayer 8 is deposited, carry out opening of the contact hole 9, form a wiring layer 10, and, finally form a protective coat 11.
[0007]
[Problem(s) to be Solved by the Invention] However, also in the conventional Salicide type MOSFET described above, there are the following problems as gate length will become still shorter from now on. First, also at the silicide-ized gate, resistance of the gate comes to check the high-speed operation of a circuit as gate length becomes short with 0.3 micrometers, 0.2 micrometers, and 0.1 micrometers. That is, the gate length of 0.2 micrometers, and the gate width of 20 micrometers, if sheet resistance of silicide is usually made into 5ohm/**, it becomes 500-ohm resistance only at the gate of 20-micrometer width of face, and it will become sufficiently large and will become the degradation factor of the high-speed operation of a circuit from the on resistance (if it carries out inmA [20 micrometer width of face and / 0.6 //micrometer] 170ohms) of MOSFET of 0.2-micrometer time.
[0008] Moreover, even if it becomes impossible for sheet resistance of the source drain field where it is not Salicide-ized under the sidewall to ignore and this is Salicide type MOSFET, it becomes the cause which lowers current driving force. this invention loses increase of the gate resistance which the gate size described above follows on being reduction-ized, and aims at offering Salicide type MOSFET which can plan high-speed operation of a circuit, and its manufacture method.
[0009]
[Means for Solving the Problem] this invention prepares the refractory-metal silicide in which the both-sides side of a gate electrode is formed in part at least in (A) Salicide type MOSFET, in order to attain the above-mentioned purpose. Furthermore, the refractory-metal silicide in which the lower part of the sidewall insulator layer of the aforementioned gate electrode is formed in part at least is prepared.
[0010] (B) Moreover, the process which deposits an oxide film on the whole surface after gate electrode formation in the manufacture method of Salicide type MOSFET, The process which deposits a nitride on the whole surface and forms a nitride sidewall by anisotropic etching, The process which **********s so that a part of both-sides side of the aforementioned gate electrode may expose the aforementioned oxide film and a part of silicon substrate under a nitride sidewall may be exposed, It is made to give the process which deposits a refractory metal on the whole surface, and the process which performs a silicide-ized reaction and removes an unreacted refractory metal.
[0011] (C) Furthermore, be made to give the process which deposits an insulator layer on the whole surface, the process

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TECHNICAL FIELD

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[Translation done.]

PRIOR ART

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* NOTICES *

EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, since a part of gate electrode both-sides side [at least] is silicide-ized according to this invention even when a gate size is reduction-ized with high integration as explained in detail, low resistance-ization of a gate electrode can be attained. Furthermore, a part of bottom of a nitride sidewall can also be silicide-ized, and the parasitism resistance under a sidewall can be reduced. And since a refractory metal becomes thin, so that the bottom of a nitride sidewall approaches a gate electrode side since the refractory metal is deposited by the wraparound at the time of sputtering so that it goes to the back that is, and it becomes so shallow that the junction depth of a source drain and high impurity concentration also approach a gate electrode side, a junction leakage current can be reduced.
[0025] moreover, between a nitride sidewall and gate electrodes and a nitride sidewall, and a silicon machine -- since the etching removal of the oxide film on a gate electrode front face and the front face of a silicon substrate used as a source drain can be certainly carried out while about 1000A **********s a wooden floor, the stable silicide formation is attained Furthermore, in the manufacture method in a view 3, since it has at an easy process and a part of gate electrode both-sides side [at least] is silicide-ized, low resistance-ization of a gate electrode can be attained.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, also in the conventional Salicide type MOSFET described above, there are the following problems as gate length will become still shorter from now on. First, also at the silicide-ized gate, resistance of the gate comes to check the high-speed operation of a circuit as gate length becomes short with 0.3 micrometers, 0.2 micrometers, and 0.1 micrometers. That is, the gate length of 0.2 micrometers, and the gate width of 20 micrometers, if sheet resistance of silicide is usually made into 5ohm/**, it becomes 500-ohm resistance only at the gate of 20-micrometer width of face, and it will become sufficiently large and will become the degradation factor of the high-speed operation of a circuit from the on resistance (if it carries out inmA [20 micrometer width of face and / 0.6 //micrometer] 170ohms) of MOSFET of 0.2-micrometer time.

[0008] Moreover, even if it becomes impossible for sheet resistance of the source drain field where it is not Salicide-ized under the sidewall to ignore and this is Salicide type MOSFET, it becomes the cause which lowers current driving force. this invention loses increase of the gate resistance which the gate size described above follows on being reduction-ized, and aims at offering Salicide type MOSFET which can plan high-speed operation of a circuit, and its manufacture method.

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MEANS

[Means for Solving the Problem] this invention prepares the refractory-metal silicide in which the both-sides side of a gate electrode is formed in part at least in (A) Salicide type MOSFET, in order to attain the above-mentioned purpose. Furthermore, the refractory-metal silicide in which the lower part of the sidewall insulator layer of the aforementioned gate electrode is formed in part at least is prepared.

[0010] (B) Moreover, the process which deposits an oxide film on the whole surface after gate electrode formation in the manufacture method of Salicide type MOSFET, The process which deposits a nitride on the whole surface and forms a nitride sidewall by anisotropic etching, The process which **********s so that a part of both-sides side of the aforementioned gate electrode may expose the aforementioned oxide film and a part of silicon substrate under a nitride sidewall may be exposed, It is made to give the process which deposits a refractory metal on the whole surface, and the process which performs a silicide-ized reaction and removes an unreacted refractory metal.

[0011] (C) Furthermore, be made to give the process which deposits an insulator layer on the whole surface, the process which etches until a part of gate electrode both-sides side is exposed with anisotropic etching, the process which deposits a refractory metal on the whole surface, and the process which performs a silicide-ized reaction and removes an unreacted refractory metal after gate electrode formation in the manufacture method of Salicide type MOSFET.

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OPERATION

[Function] As described above, even when a gate size is reduction-ized with high integration according to this invention, since [of a gate electrode] a part of both-sides side is silicide-ized at least, low resistance-ization of a gate electrode can be attained. Moreover, since a part of sidewall is removed and silicide-ization on a source drain was close brought to near the gate, the parasitism resistance under a sidewall can be reduced.
[0013] And in the above (B), since a refractory metal becomes thin, so that the bottom of a nitride goes to a gate electrode side since it is made to deposit a refractory metal by the wraparound at the time of sputtering so that it goes to the back that is, and it becomes so shallow that the junction depth of a source drain and high impurity concentration also approach a gate electrode side, a junction leakage current can be reduced.
[0014] moreover, the above (B) -- setting -- between a nitride sidewall and gate electrodes and a nitride sidewall, and a silicon machine -- since the etching removal of the oxide film on a gate electrode front face and the front face of a silicon substrate used as a source drain can be certainly carried out while about 1000A **********s a wooden floor, the stable silicide formation is attained

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[Translation done.]

EXAMPLE

[Example] Hereafter, it explains in detail, referring to drawing about the example of this invention. Drawing 1 is the manufacturing process cross section of Salicide type MOSFET showing the 1st example of this invention. Here, the example of N channel MOSFET shows.

(1) First, as shown in drawing 1 (a), form the field oxide film 22 (about 4000A) by the usual LOCOS method on the P type silicon substrate 21. Then, the gate oxide film 23 (about 100A) is formed, and about 3000A of polycrystal silicon films 24 used as a gate electrode is further deposited by LPCVD. The usual HOTORISO etching performs pattern formation of a gate electrode. 25 is a LDD layer.

[0016] (2) Next, as shown in drawing 1 (b), deposit 300A - about 700A of oxide films 26 on the whole surface by LPCVD. in this case, lowering temperature as membrane formation conditions etc. -- as ****** -- a next process -- it considers as the membraneous quality to which etching progresses sufficiently more quickly than the field oxide film 22 at the time of the oxide-film wet etching in (4 [refer to drawing 1 (d)]) Then, the about 1500A nitride 27 is deposited by plasma CVD. in this case, lowering RF power as membraneous quality etc. -- low -- it is necessary to consider as stress membraneous quality and to prevent that a defect enters into silicon

[0017] (3) Next, as shown in drawing 1 (c), by anisotropic etching, ********** a nitride 27 and form the sidewall 28 with width of face of about 1500A. Then, a sidewall 28 is used as a mask, impurity pouring for source drain formation is performed into silicon, and the source drain layer 29 is formed.

(4) next, it is shown in drawing 1 (d) -- as -- the etchant of a fluoric acid system -- the aforementioned process -- carry out etching removal of the oxide film 26 deposited in (2 [refer to drawing 1 (b)]), and carry out etching removal also of the polycrystal silicon film 24 which constitutes a gate electrode under the nitride sidewall 28 further, and about 1000A also of the oxide films of the pinched portion Then, about 300-400A of high-melting point metal membranes 30, such as Ti, is deposited on the whole surface by sputtering. It is made for the high-melting point metal membrane 30 to accumulate also on the bottom of a gate both-sides side and the nitride sidewall 28 enough in this case by sputtering, such as high 875MHzx double precision of an efficient consumer response resonance frequency.

[0018] (5) Next, as shown in drawing 1 (e), by annealing, make silicide-ization cause in the portion which the high-melting point metal membrane 30, the P type silicon substrate 21, and the polycrystal silicon film 24 contacted, and consider as refractory-metal silicide 31. Furthermore, etching removes alternatively the unreacted refractory metal on an oxide film 26 and a nitride 27. Then, low resistance-ized annealing of refractory-metal silicide 31 is performed.

[0019] (6) Next, as shown in drawing 1 (f), according to the usual method, deposit an interlayer 32, open the contact hole 33 with wiring, and carry out patterning of the wiring layer 34 there. Drawing 3 is the manufacturing process cross section of Salicide type MOSFET showing the 2nd example of this invention.

[0020] (1) First, as shown in drawing 3 (a), complete to gate patterning like drawing 1 (a). That is, the field oxide film 42 (about 4000A) is formed by the usual LOCOS method on the P type silicon substrate 41. Then, the gate oxide film 43 (about 100A) is formed, and about 3000A of polycrystal silicon films 44 used as a gate electrode is further deposited by LPCVD. The usual HOTORISO etching performs pattern formation of a gate electrode. 45 is a LDD layer.

[0021] (2) Next, as shown in drawing 3 (b), deposit about 1000A of oxide films 46 on the whole surface by LPCVD. in this case, lowering temperature as membrane formation conditions etc. -- as ****** -- a next process -- it considers as the membraneous quality to which etching progresses sufficiently more quickly than the field oxide film 42 at the time of the oxide-film anisotropic etching in (3 [refer to drawing 1 (c)])

(3) Subsequently, advance etching until it **********s the oxide film 46 by anisotropic etching and about 1000A of oxide films 47 comes out to the both-sides side of the gate further, as shown in drawing 3 (c).

[0022] (4) Subsequently, as shown in drawing 3 (d), deposit a refractory metal 48 on the whole surface. In this case, the sputtering technology which a refractory metal 48 deposits on the both-sides side of the gate enough is used like the 1st example.

(5) Next, as shown in drawing 3 (e), perform silicide-ized reaction, unreacted refractory-metal removal, and low resistance-ized annealing like drawing 1 (e). That is, by this annealing, silicide-ization is made to cause in the portion in contact with the polycrystal silicon film 44 which are the high-melting point metal membrane 48, the P type silicon substrate 41, and a gate electrode, and it considers as refractory-metal silicide 49.

[0023] The following follows the process of drawing 1 (f). In addition, it is desirable to perform deposition of the

aforementioned refractory metal with sputtering technology with sufficient step coverages, such as a resonance frequency (for high frequency to be used) and efficient consumer response sputtering technology. Moreover, this invention is not limited to the above-mentioned example, and based on the meaning of this invention, various deformation is possible for it and it does not eliminate these from the range of this invention.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the manufacturing process cross section of Salicide type MOSFET showing the 1st example of this invention.
[Drawing 2] It is the manufacturing process cross section of the conventional Salicide type MOSFET.
[Drawing 3] It is the manufacturing process cross section of Salicide type MOSFET showing the 2nd example of this invention.
[Description of Notations]
21 41 P type silicon substrate
22 42 Field oxide film
23 43 Gate oxide film
24 44 Polycrystal silicon film (gate electrode)
25 45 LDD layer
26, 46, 47 Oxide film
27 Nitride
28 Sidewall
29 Source Drain Layer
30 48 High-melting point metal membrane
31 49 Refractory-metal silicide
32 Interlayer
33 Contact Hole
34 Wiring Layer

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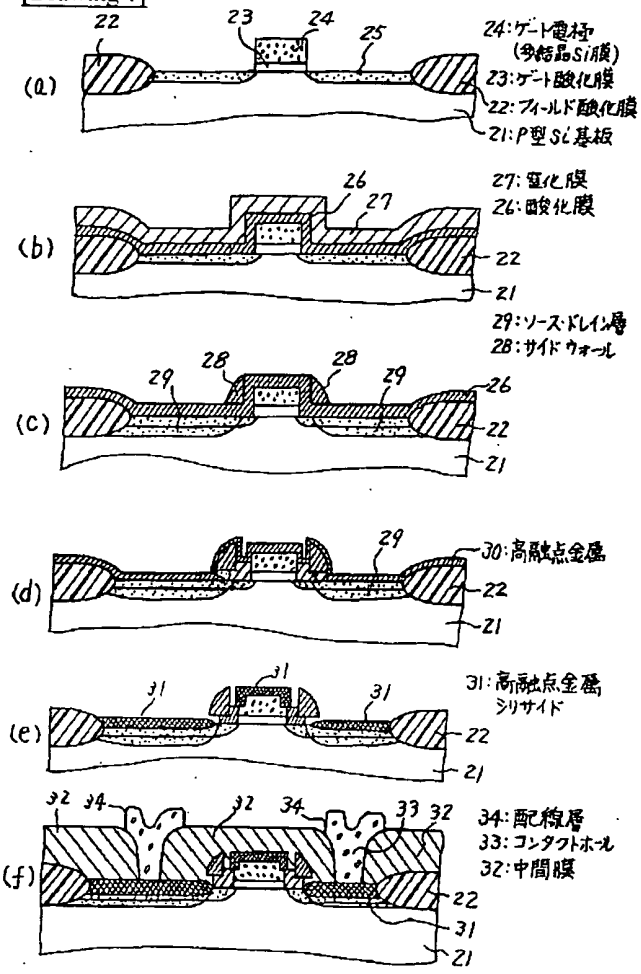
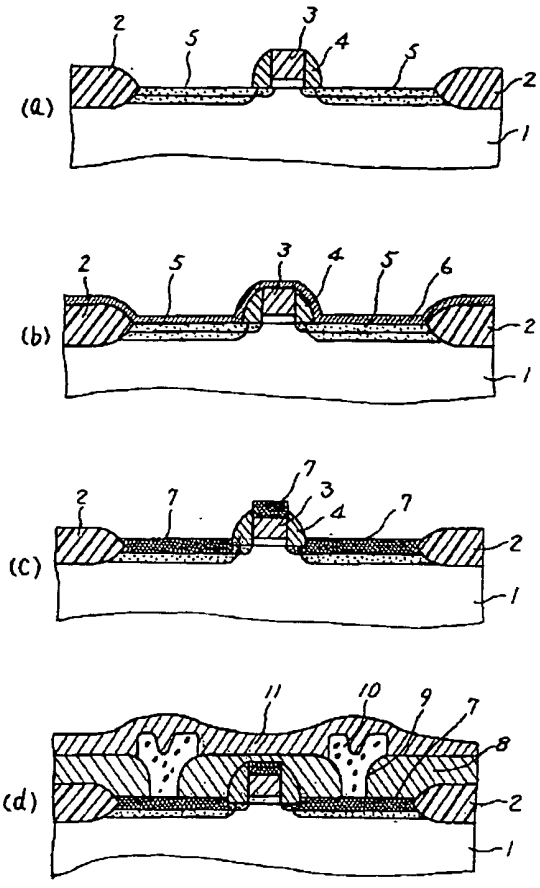
DRAWINGS

[Drawing 1]



[Drawing 2]


(a)
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(b)
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2
7
7
3
4
7
2
1
(d)
11
10
9
7
8
2
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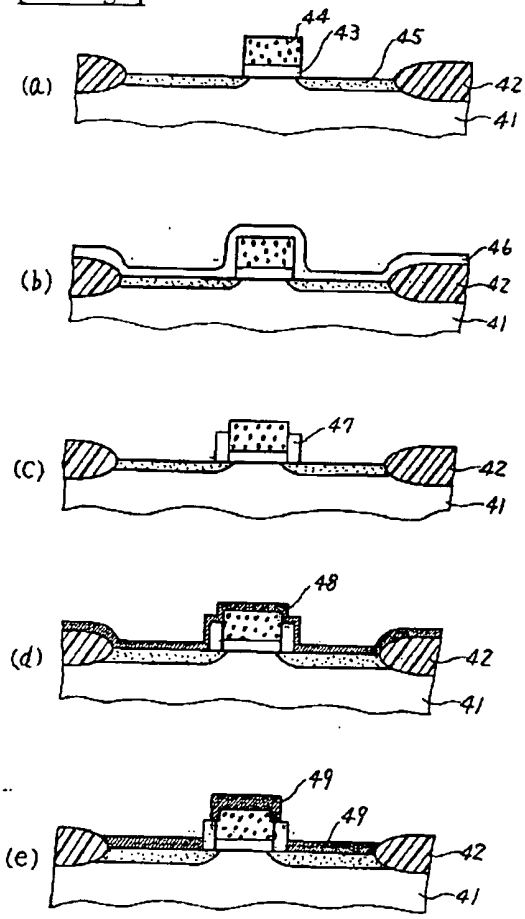
[Drawing 3]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(e)
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which etches until a part of gate electrode both-sides side is exposed with anisotropic etching, the process which deposits a refractory metal on the whole surface, and the process which performs a silicide-ized reaction and removes an unreacted refractory metal after gate electrode formation in the manufacture method of Salicide type MOSFET.

[0012]

[Function] As described above, even when a gate size is reduction-ized with high integration according to this invention, since [of a gate electrode] a part of both-sides side is silicide-ized at least, low resistance-ization of a gate electrode can be attained. Moreover, since a part of sidewall is removed and silicide-ization on a source drain was close brought to near the gate, the parasitism resistance under a sidewall can be reduced.

[0013] And in the above (B), since a refractory metal becomes thin, so that the bottom of a nitride goes to a gate electrode side since it is made to deposit a refractory metal by the wraparound at the time of sputtering so that it goes to the back that is, and it becomes so shallow that the junction depth of a source drain and high impurity concentration also approach a gate electrode side, a junction leakage current can be reduced.

[0014] moreover, the above (B) -- setting -- between a nitride sidewall and gate electrodes and a nitride sidewall, and a silicon machine -- since the etching removal of the oxide film on a gate electrode front face and the front face of a silicon substrate used as a source drain can be certainly carried out while about 1000A **********s a wooden floor, the stable silicide formation is attained

[0015]

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[0023] The following follows the process of drawing 1 (f). In addition, it is desirable to perform deposition of the aforementioned refractory metal with sputtering technology with sufficient step coverages, such as a resonance frequency (for high frequency to be used) and efficient consumer response sputtering technology. Moreover, this invention is not limited to the above-mentioned example, and based on the meaning of this invention, various deformation is possible for it and it does not eliminate these from the range of this invention.

[0024]

[Effect of the Invention] As mentioned above, since a part of gate electrode both-sides side [at least] is silicide-ized according to this invention even when a gate size is reduction-ized with high integration as explained in detail, low resistance-ization of a gate electrode can be attained. Furthermore, a part of bottom of a nitride sidewall can also be silicide-ized, and the parasitism resistance under a sidewall can be reduced. And since a refractory metal becomes thin, so that the bottom of a nitride sidewall approaches a gate electrode side since the refractory metal is deposited by the wraparound at the time of sputtering so that it goes to the back that is, and it becomes so shallow that the junction depth of a source drain and high impurity concentration also approach a gate electrode side, a junction leakage current can be reduced.

[0025] moreover, between a nitride sidewall and gate electrodes and a nitride sidewall, and a silicon machine -- since the etching removal of the oxide film on a gate electrode front face and the front face of a silicon substrate used as a source drain can be certainly carried out while about 1000A **********s a wooden floor, the stable silicide formation is attained Furthermore, in the manufacture method in a view 3, since it has at an easy process and a part of gate electrode both-sides side [at least] is silicide-ized, low resistance-ization of a gate electrode can be attained.

[Translation done.]